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Examiner Name	Wamsley, P.
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Attorney Docket No. PD-99W192

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ostrow et al

Serial No. 10/046,871

Filed: 01/15/2002

For: STATISTICALLY BASED CASCADED ANALOG-TO-DIGITAL CONVERTER CALIBRATION TECHNIQUE

Art Unit: 2819

Examiner: P. Wamsley

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Office Action mailed April 4, 2003.

Drawings

The drawings stand objected to, on the grounds that FIGS. 3A-8B should be designated by a legend such as "Prior Art" since allegedly only that which is old is illustrated. The Examiner asserts that "the present invention appears only in Figure 9." The objection is respectfully traversed.

The Examiner asserts that FIGS. 3A-8B are prior art, but provides no reasoning or basis for the assertion that only that which is old is shown. Applicants have not conceded that these figures illustrate only that which is old. For this reason alone, the objection should be withdrawn.

FIGS. 3A-3B illustrate output waveforms for the digital and analog outputs of stages 1 and 2 of FIGS. 1 and 2, for an input signal swept over the ADC full scale voltage range. See specification at 4:12-23. There is no discussion that FIGS. 3A-3B illustrate only that which is known. The discussion of the probability density function of digital output bits at 4:24 to 5:2 is not described as that which is already known. The specification states, at 5:3-5, that "the calculation of bit probability density function as described above can be used in the context of calibration of an analog-to-digital converter." FIGS. 4A-8B are used in explanation of this calibration technique.

FIG. 9 is an exemplary hardware implementation of an N-bit ADC embodying aspects of the invention, which implements the techniques described with respect to FIGS. 3A-8B.

Because the Examiner has failed to provide reasons as to why FIGS. 3A-8B illustrate only that which is known, and because these figures illustrate features of the inventive techniques, the objection to the drawings should be withdrawn.

Claims Rejection - 35 USC 103

Claims 1-13 stand rejected as being unpatentable over the "Admitted Prior Art" (APA) in view of Kasson et al. (Kasson). The rejection is respectfully traversed, on the grounds that a prima facie case of obviousness has not been established.

The office action notes that when applicant states that something is prior art, it is taken as being available as prior art against the claims. Applicants do not disagree with this general statement. However, applicants deny that the APA in this case extends to the matters asserted by the Examiner as constituting APA.

FIGS. 1 and 2 of applicants' specification show known ADC circuits, and are labeled with the legend "Prior Art." Applicants have never stated that FIGS. 3A-8B illustrate the prior art, and have denied that this is so in the above section addressing the requirement to label these figures as prior art. The analyses of bit statistics of FIGS. 4A-8B are clearly not discussed as being known in the art.

The Examiner states that "APA provides a calibration method comprising the steps of applying an input signal to an analog to digital converter, hereafter ADC; determining at least one error value; and using that value for each stage for compensation." Applicants deny that the APA provides such a calibration method. In fact, no known calibration method is described in applicants' specification for the ADC circuits shown in FIGS. 1 and 2.

The Examiner further states that ADC provides an ADC comprising a calibration circuit and an error compensation circuit. Applicants respectfully disagree, and deny that the APA provides an ADC comprising such circuits. The circuits of FIGS. 1 and 2 do not include a calibration circuit or an error compensation circuit.

The Examiner concedes that the APA does not "teach application of a signal having a symmetric or uniform probability density." Kasson is cited as allegedly showing injection of a controlled signal in the form of a symmetric triangle wave. The Examiner alleges that it would have been obvious to have applied Kasson's teachings to APA, on the rationale that one of ordinary skill in the art would have been motivated

to use a symmetric triangle wave to reduce channel crosstalk and quantizing error noise, as suggested by Kasson on column 3. Applicants respectfully disagree.

Kasson describes a technique for adding and subsequently subtracting a deterministic dither signal in the context of a digital transmission system. Kasson does not teach or suggest a method for calibrating an ADC. Rather, Kasson adds and subsequently subtracts via filtering a small deterministic dither signal whose purpose is to improve the signal-to-noise ratio of the overall system when the analog input signal is of very small amplitude, for example, a few Least Significant Bits or LSBs, relative to the full scale dynamic range of the system. The controlled signal of Kasson is applied during normal operation of the system, not during a calibration method. Kasson does not determine an error value for each stage of the ADC resulting from application of a signal having a symmetric or uniform probability density property to the ADC analog input.

Claim 1 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

[A] applying a signal having a symmetric or uniform probability density property to the ADC analog input;

[B] determining at least one error value for each stage resulting from application of said signal;

[C] using the at least one error value for each stage to compensate each of said n stages during ADC operation.

The reference characters [A], [B] and [C] have been added for convenience in reference.

The APA of FIGS. 1-2 does not teach or suggest any of paragraphs A, B or C of Claim 1.

Kasson does not teach at least the features of paragraphs B and C of Claim 1.

There is in any event no suggestion or motivation to combine the APA of FIGS. 1-2 with Kasson to arrive at the invention of Claim 1. Even if the signal of Kasson is fed into the ADC of FIG. 1, the claimed invention still does not result.

The rejection of Claim 1 and the claims depending therefrom should be withdrawn.

The Examiner states, regarding Claims 3 and 13, that APA examines statistics of bit transitions. Applicants respectfully disagree that the APA includes this feature. The description of examination of statistics of bit transitions in the application was in the context of describing applicants' invention, not the APA of FIGS. 1-2.

The Examiner further alleges, regarding Claim 5, that APA determines deviation from an ideal transfer function, citing applicants' specification at 5:3, thereby correcting gain and offset errors, and that, regarding Claim 6, the APA uses this deviation to determine error values. Applicants deny that APA includes these features. The circuits of FIGS. 1-2 are prior art, but the description of the calculation of bit probability density function at 5:3 pertains to applicants' innovation, not a description of that which is known.

The additional allegations regarding the APA status of features of Claims 7, 8, 11, 12 are also traversed. Each of the allegations is supported only by applicants' description of aspects of their innovation, not of features admitted to be prior art.

Claim 9 is drawn to an analog-to-digital converter (ADC), comprising:

a cascade of N-stages, wherein a first stage determines the most significant or coarse bit(s) for the ADC, and a last stage determines the least significant or finest resolution bit(s) for the ADC, the cascade of N-stages forming a composite n-bit ADC transfer function;

an ADC analog input port;

an ADC digital output port;

the first stage having a stage analog input connected to the ADC analog input port, and producing a first stage digital output and a first stage digital output;

a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, the calibration circuit for determining at least one error value for each stage resulting from application of said signal;

an error compensation circuit coupled to the calibration circuit for compensating each stage in response to said at least one error value for each stage.

The APA of FIGS. 1 and 2 does not describe or teach a calibration circuit or an error compensation circuit as recited in Claim 9.

Kasson does not teach or suggest a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, which

determines at least one error value for each stage resulting from application of the signal. Nor does Kasson teach or suggest an error compensation circuit coupled to a calibration circuit for compensating each state in response to the at least one error value for each stage.

Because the APA and Kasson alone or in combination do not teach or suggest all claim limitations, the rejection of Claim 9 as well as the rejection of the claims depending therefrom should be withdrawn.

Claim 13 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the n stages including a first stage which determines the most significant or coarse bit(s), and a last stage which determines the least significant or finest resolution bit(s), the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

[A] applying a signal having a symmetric or uniform probability density property to the ADC analog input;

[B] determining at least one error value for each stage resulting from application of said signal, by examining statistics of bit transitions at each stage to compute bit transition probability density functions for both individual stage outputs and for logical combinations of the stage outputs to determine deviation from a desired transfer function related to both gain and offset errors within and between the stages;

[C] using the at least one error value for each stage to compensate each of said n stages during ADC operation.

The APA of FIGS. 1-2 does not describe or suggest any of the limitations of Claim 13. Kasson does not teach or suggest at least the limitations of paragraphs B and C of Claim 13. For these reasons, the invention of Claim 13 is not taught or suggested by the APA or Kasson, alone or in combination.

CONCLUSION

The outstanding objection and rejection have been addressed, and the application is in condition for allowance. Such favorable reconsideration is solicited.

Respectfully submitted,

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